IN THE CLAIMS:

Please cancel claim 1 without prejudice or disclaimer, and amend claims 2-7 as follows:

1. (Cancelled)

2. (Currently Amended) A logic verification system comprising:

a logic simulation accelerator including:

a ~~device~~ logic simulator operating on a general purpose processor;

a device including a programmable ~~logic device using~~ EPGA module composed by FPGAs; and

a bridge circuit ~~for transmitting and receiving~~ which selectively transmits and receives corresponding data between said ~~device~~ logic simulator operating on said general purpose processor and ~~said device including the programmable logic device using~~ said FPGA[[s]] module according to designed functions assigned to said EPGAs for each of a plurality of designed logic circuits,

wherein [[when]] all pins of the FPGA module used in [[the]] a verification process for verifying one of said plurality of designed logic circuits by [[in]] said logic simulator ~~emulator and the bridge circuit~~ are wired in direct to the bridge circuit ~~for all pins of said FPGA module and the~~ to accelerate logic simulation ~~is accelerated~~, [[the]] a cutting end of [[the]]a verification logic of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module, and [[the]] a correspondence between each pin of the external interface connector of said FPGA module and a logic signal is ~~performed~~ established on said logic simulator on said general purpose processor.

3. (Currently Amended) The logic verification system according to claim 2, wherein the verification logic implemented ~~mounted~~ on said FPGA module is provided with a means for transmitting a direction control signal of a two-way signal controlled therewith to the bridge circuit using an interface.

4. (Currently Amended) The logic verification system according to claim 2, ~~wherein~~ further comprising a means for automatically detecting a signal direction of a two-

way signal between said FPGA module and ~~the device mounting~~ the bridge circuit ~~is provided~~, and [[the]] program data of the same FPGA module ~~group mounting the~~ implementing different verification ~~object~~ logics is used in ~~a couple of~~ verification processes consisting of [[the]] acceleration of logic simulation and logic emulation for the plurality of designed logic circuits.

5. (Currently Amended) The logic verification system according to claim 4, wherein said means for automatically detecting the signal direction of the two-way signal ~~between said devices is capable of setting~~ sets a drivability level of output circuits of ~~both devices~~ the EPGA module and the bridge circuit and giving [[the]] a priority in determination of signal direction to one of the ~~device~~ EPGA module and the bridge circuit having higher drivability.

6. (Currently Amended) The logic verification system according to claim 4, further comprising: ~~a means for automatically detecting the signal direction of a two-way signal between said FPGA module and the device mounting the bridge circuit; and~~ a means for inputting the signal direction of the two-way signal to the logic simulator on the general purpose processor,

wherein [[the]] a disagreement between a signal direction of the logic simulator and ~~a disagreement of~~ a signal direction [[in]] of the FPGA module is detected by comparing said [[two]] signal directions.

7. (Currently Amended) The logic verification system according to claim 6, wherein said means for automatically detecting the signal direction of the two-way signal ~~between said devices is capable of setting~~ sets a drivability level of output circuits of ~~both devices~~ the EPGA module and the bridge circuit and giving the priority in determination of signal direction [[ot]] to one of the ~~device~~ EPGA module and the bridge circuit having higher drivability.